What is claimed is:

1. A semiconductor device comprising:

a semiconductor layer;

a gate insulator provided on the semiconductor layer;

a gate electrode provided on the gate insulator;

a source region and a drain region, which are of a first conductivity type and are provided in the semiconductor layer on both sides of the gate electrode in plan view;

a cap layer, a channel region, and an under-channel region which are provided in the semiconductor layer between the source region and the drain region in a descending order from an interface with the gate insulator, the under-channel region being of a second conductivity type; and

a bias electrode member for applying a voltage to the under-channel region, wherein

the channel region is formed of a first semiconductor,

the cap layer and the under-channel region are formed of a second semiconductor and a third semiconductor, respectively, each of which has a larger band gap than the first semiconductor,

the bias electrode member is capable of applying the voltage independently of the gate electrode.

2. The semiconductor device according to claim 1, wherein an absolute value of a threshold voltage is 0.2 V or

less when a voltage applied to the bias electrode member is 0 V.

3. The semiconductor device according to claim 1, wherein an impurity concentration of the under-channel region is 1×10^{18} cm^{-3} or more.

4. The semiconductor device according to claim 1, wherein when a voltage applied to the bias electrode member is near 0 V, an absolute value of a rate of change in a threshold voltage relative to a change in the voltage applied to the bias electrode member is 0.45 or more.

5. The semiconductor device according to claim 1, wherein when the bias electrode member is applied with a forward bias voltage and a reverse bias voltage which bias junctions formed between the drain region or the source region and the cap layer, between the drain region or the source region and the channel region, and between the drain region or the source region and the under-channel region in a forward direction and a reverse direction, respectively, the ratio of a rate of change in a threshold voltage relative to a change in an applied voltage under the application of the forward bias voltage to a rate of change in the threshold voltage relative to a change in the applied voltage under the application of the reverse bias voltage is 1.3 or more.

6. The semiconductor device according to claim 5, wherein said ratio is 1.318 or more.

7. The semiconductor device according to claim 1,

wherein a thickness of the cap layer is not less than 1 nm and not more than 10 nm.

8. The semiconductor device according to claim 1, wherein the first semiconductor is a semiconductor comprising SiGe as a major component, while the second and third semiconductors are each formed of Si.

9. The semiconductor device according to claim 8, wherein: the source region and the drain region have p-type conductivity; and a p-channel is formed in the channel region under a predetermined condition.

10. The semiconductor device according to claim 1, wherein the first semiconductor is a semiconductor comprising SiGeC as a major component, while the second and third semiconductors are each formed of Si.

11. The semiconductor device according to claim 10, wherein: the source region and the drain region have n-type conductivity; and an n-channel is formed in the channel region under a predetermined condition.

12. The semiconductor device according to claim 11, wherein the under-channel region is doped with boron.

13. The semiconductor device according to claim 1, wherein an insulating layer is provided under the semiconductor layer.

14. A complementary semiconductor device comprising a first semiconductor device and a second semiconductor device, each of which is formed of the semiconductor device according

to claim 1:wherein

in the first semiconductor device, the source region and the drain region have p-type conductivity and a p-channel is formed in the channel region under a predetermined condition; and

in the second semiconductor device, the source region and the drain region have n-type conductivity and an n-channel is formed in the channel region under a predetermined condition.

15. The complementary semiconductor device according to claim 14, wherein in each of the first and second semiconductor devices, the first semiconductor is a semiconductor comprising SiGeC as a major component while the second and third semiconductors are each formed of Si.